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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/664,379	09/17/2003	Darrin Benzer	13546US02	4562

23446 7590 06/24/2005

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EXAMINER	
NGUYEN, LONG T	

ART UNIT	PAPER NUMBER
2816	

DATE MAILED: 06/24/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/664,379	BENZER ET AL.	
	Examiner	Art Unit	
	Long Nguyen	2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *06 May 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *9-24* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *9-24* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *17 September 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

1. This office action is responsive to the amendment filed on 5/6/05.

Terminal Disclaimer

2. The terminal disclaimer filed on 5/9/05 disclaiming the terminal portion of any patent granted on this application which would extend beyond the expiration date of U.S. Patent 6,650,167 has been reviewed and is accepted. The terminal disclaimer has been recorded.

Claim Objections

3. Claims 9-24 are objected to because of the following informalities:

Claim 9, line 3, "0V said" should be changed to --0V, said--.

Claims 10-15 are objected to because they include the informality of claim 9.

Claim 16, line 3, "0V" should be changed to --0V, said method---.

Claims 17-19 are objected to because they include the informality of claim 16.

Claim 20, line 6, "circuit" should be changed to --transistor device—to avoid an unclear antecedent basis between a level shifter circuit (currently recited on lines 5-6 with the level shifter circuit recited earlier on line 3).

Claim 20, line 6, "devices" should be changed to --devices, said method---.

Claims 21-24 are objected to because they include the minor informalities of claim 20.

Appropriate correction is required.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 9-24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hirano (USP 5,650,742) in view of Cress et al. (USP 6,483,386).

With respect to claims 9-15, each of Figures 1 and 31 of the Hirano reference discloses a level shifter circuit (101 in Figure 1, or 3001 in Figure 31), which meets a method of translating a voltage level of a single-ended input signal (I1 in Figure 1, I30 in Figure 31) using at least one pass NMOS transistor device (Qn101 in Figure 1, Qn3001 in Figure 31) including: outputting a first voltage level if the single-ended input signal is in a first state (i.e., if the first state of the input signal I1/I30 is at logic Lo, the output O1/O30 of the circuit is at logic Hi; and if the first state of the input signal I1/I30 is at logic Hi, the output O1/O30 of the circuit is at logic Lo); and outputting a second voltage level if the single ended input is in a second state (i.e., if the first state of the input signal I1/I30 is at logic Hi, the output O1/O30 of the circuit is at logic Lo; and if the first state of the input signal I1/I30 is at logic Lo, the output O1/O30 of the circuit is at logic Hi). The Hirano reference does not disclose that the at least one pass NMOS transistor device (Qn101 in Figure 1, Qn3001 in Figure 31) is a native NMOS transistor device having a threshold voltage less than 0V. However, the Cress et al. reference discloses (note M3 in Figure 5, lines 45-65 of Col. 2, lines 18-43 of Col. 3, and lines 4-31 of Col. 4 of Cress et al.) a pass transistor device (M3) is a native NMOS transistor device having a threshold voltage less than 0V (-200mV, see lines 34-36 of Col. 3 of Cress et al.) for the purpose of having an input signal fully passes through the pass NMOS transistor device because the use of a native NMOS as a pass transistor provides a signal with low signal distortion (see line 24-31 of Col. 4, Cress et al.).

Therefore, it would have been obvious to one having skill in the art at the time the invention was made to modify each of the circuits in Figures 1 and 31 of the Hirano reference by specifically using the native NMOS pass transistor (M3) having a threshold voltage of less than 0V, as taught by the Cress et al. reference, for the NMOS pass transistor (Qn101 in Figure 1, or Qn3001 in Figure 31 of Hirano) for the purpose of reducing noise and improving the performance of the circuitry since native NMOS pass transistor provides a signal with low distortion. Thus, each of the modifications (Figure 1 and Figure 31) meets all the limitations of these claims including the limitation that the at least one native NMOS transistor device having a threshold voltage less than 0V (-200mV as discussed above).

With respect to claim 16, each of the above modifications of the level shifter circuit as discussed above (with regard to claim 9) meets all the limitation of this claim, i.e., the modification circuit discloses a level shifter circuit (101 in Figure 1, or 3001 in Figure 31), which meets a method of translating a voltage level of a single-ended input signal (I1/I30) using at least one native NMOS transistor device having a threshold voltage less than 0V (-200mv, see rejection of claim 9) including: determining if the input signal (I1/I30) is high (input signal I1/I30 having logic Hi, transistor Qn102 turns ON); outputting a low signal if the input signal is high (output signal O1/O30 is a low signal if the input signal I1/I30 is high); and outputting a high signal if the input signal is not high (Qn102 is off and Qp102 is ON for Figure 1, and Qn2002 is off and Qp3002 is ON for Figure 31).

With respect to claim 17, each of the above modifications meets the limitation that determining if the input signal is high includes determining if the input signal (I1/I30) is greater than a first voltage (the threshold voltage of the n-channel transistor Qn102 in Figure 1, or the

threshold voltage of the n-channel transistor Qn3002 in Figure 31, i.e., the input signal I1/I30 is considered to be Hi when the input signal I1/I30 is greater than the threshold voltage of the enhancement n-channel transistor Qn102 or Qn3002).

With respect to claim 18, each of the above modifications meets the limitation that determining if the input signal (I1/I30) is not high includes determining if the input signal is less than a second voltage (the threshold voltage of the p-channel transistor Qp102 in Figure 1 of Qp3002 in Figure 31, i.e., the input signal I1/I30 is considered to be Lo when the input signal I1/I30 is less than the threshold voltage of the enhancement p-channel transistor Qp102 or Qp3002, so transistor Qp102 or Qp3002 is ON).

With respect to claim 19, each of the above modifications meets the limitation that eliminating static current drain (the feedback transistor Qp101 in Figure 1 of the Hirano reference in the above modification, see lines 58-65 of Col. 7 of the Hirano reference, or the feedback transistor Qp3001 in Figure 31 of the Hirano reference in the above modification).

With respect to claims 20-24, each of the above modifications (as discussed above with regard to claim 9) meets all the limitations of these claims, i.e., the level shifter circuit having a single-end input (I1/I30), a first native NMOS transistor (the replacement of the Qn101 in Figure 1 or Qn3001 in Figure 31 as discussed in claim 9) having threshold voltage of less than 0V (-200mV, see discussion in claim 9), a second transistor (Qn102 in Figure 1, or Qn3002 in Figure 31), and a level shifter transistor (Qp102 in Figure 1 or Qp3002 in Figure 31). Note that the method steps recited in this claim are also met including: determining if the input signal is greater than a threshold value of the second transistor (Qn102 in Figure 1 or Qn3002 in Figure 31 turns ON if input signal I1 or I30 is greater than threshold value of Qn102 or Qn3002,

respectively); outputting a low signal if the input signal is greater than the threshold value (Qn102 or Qn3002 turns ON if input signal I1 or I30 is greater than threshold value of Qn102 or Qn3002, respectively, so output O1/O30 is Lo and having a ground voltage level); outputting a Hi signal if the input signal is not greater than the threshold value (if input signal I1 or I30 is not greater than threshold value of Qn102 or Qn3002, respectively, then Qp102 or Qp3002 turns ON respectively so output O1/O30 is Hi and having a VDD level); and eliminating static current drain (by feed back transistor Qp101 in Figure 1, or Qp3001 in Figure 31); and wherein outputting a high signal comprising determining if the input signal is "greater" than a second threshold value (the threshold of Qp102 or Qp3002 because if the input I1 or I30 is greater than the threshold of Qp102 or Qp3002, respectively, then Qp102 or Qp3002 turns off; note that Qp102 or Qp3002 turns On when I1 or I30 is less than the threshold of Qp102 or Qp3002, respectively); and determining if the input signal is less than the threshold value but greater than the second threshold value (the output signal is not determined Hi or Lo).

Response to Arguments

6. Applicant's arguments filed on 5/9/05 have been fully considered but they are not persuasive.

Applicant argues that the Hirano reference does not discloses/teaches that the circuit of Figure 1 is not a single ended input circuit receiving a single ended input signal. However, this argument is not persuasive because the circuit 101 in Figure 1 is a single ended input circuit because the circuit 101 receives a singled ended input signal I1. Note that the signal S1 is a control signal for the circuit, not an input signal, i.e., the circuit 101 in Figure 1 receives only one input data signal (namely I1), and the signal S1 is the control signal to control transistor Qn101

of the circuitry. Further, the newly added limitation "single ended input circuit" is also clearly met as shown in Figure 31 of Hirano.

Applicant argues that the office action does not provide any motivation to combine Hirano and Cress. However, this argument is not persuasive because the motivation was provided the use of NMOS native transistor as a pass transistor provides a signal with low distortion and thus it will reduces noise and improve the performance of the circuitry.

In response to applicant's argument that there is no suggestion to combine the references, the examiner recognizes that obviousness can only be established by combining or modifying the teachings of the prior art to produce the claimed invention where there is some teaching, suggestion, or motivation to do so found either in the references themselves or in the knowledge generally available to one of ordinary skill in the art. See *In re Fine*, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988)and *In re Jones*, 958 F.2d 347, 21 USPQ2d 1941 (Fed. Cir. 1992). In this case, the primary reference (Hirano) teaches all the limitations of the claims except that the NMOS pass transistor is a native NMOS pass transistor having threshold voltage less than 0V. The secondary reference (Cress et al.) teaches that the use of NMOS native transistor as a pass transistor having advantage of providing a signal with low distortion and thus it is obvious to one having ordinary skill in the art to use NMOS native transistor for the NMOS pass transistor for the purpose of reducing noise and improving the performance of the circuitry.

Conclusion

7. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

8. Any inquiry concerning this communication or earlier communications from the examiner should be directly to Examiner Long Nguyen whose telephone number is (571) 272-1753. The Examiner can normally be reached on Monday to Friday from 8:30am to 5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tim Callahan, can be reached at (571) 272-1740. The fax number for this group is (703) 872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

June 23, 2005

LONG NGUYEN
PRIMARY EXAMINER